METHOD FOR MANUFACTURING MTJ CELL OF MAGNETIC RANDOM ACCESS MEMORY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for fabricating a MTJ cell of a magnetic random access memory (hereinafter, referred to as 'MRAM'), having a higher speed than a SRAM, integration density as high as a DRAM, and a property of a nonvolatile memory such as a flash memory.

2. Description of the Prior Art

Most of the semiconductor memory manufacturing companies have developed the MRAM using a ferromagnetic material as one of the next generation memory devices.

The MRAM is a memory device for reading and writing information. It has multi-layer ferromagnetic thin films, and operates by sensing current variations according to a magnetization direction of the respective thin film. The MRAM has high speed and low power consumption, and allows high integration density due to the special properties of the magnetic thin film. The MRAM also performs a nonvolatile memory operation similar to a flash memory.

The MRAM is a memory device which uses a giant

magneto resistive (GMR) phenomenon or a spin-polarized magneto-transmission (SPMT) generated when the spin influences electron transmission.

The MRAM using the GMR utilizes the phenomenon that resistance is remarkably varied when spin directions are different in two magnetic layers having a non-magnetic layer therebetween to implement a GMR magnetic memory device.

The MRAM using the SPMT utilizes the phenomenon that larger current transmission is generated when spin directions are identical in two magnetic layers having an insulating layer therebetween to implement a magnetic permeable junction memory device.

The MRAM comprises a transistor and a MTJ cell, a diode and a MTJ cell, and a MTJ cell.

Fig. 1 is a cross-sectional diagram illustrating a MTJ cell structure of a conventional MRAM.

Referring to Fig. 1, a lower insulating layer 11 is formed on a semiconductor substrate (not shown). The lower insulating film 11 is an insulating film planarizing the entire surface of the semiconductor substrate having a device isolation film (not shown), a transistor (not shown) comprising a first wordline which is a read line and a source/drain region, a ground line (not shown), a

conductive layer (not shown), and a second wordline (not shown) which is a write line thereon.

Next, a connection layer 13 electrically connected to the conductive layer is formed using Ta.

A pinned ferromagnetic layer 15 electrically connected to the connection layer 13 is then formed.

The pinned ferromagnetic layer 15 includes a stacked structure of a NiFe layer, a PtMn layer, a CoFe layer, a Ru layer and a CoFe layer.

Thereafter, a tunnel barrier layer 17 is formed on the pinned ferromagnetic layer 15.

Here, the tunnel barrier layer 17 is formed using Al_2O_3 and has a thickness of less than 2nm which is the minimum thickness required for data sensing.

A free ferromagnetic layer 19 is then formed on the tunneling oxide film 17.

The free ferromagnetic layer 19 includes a stacked structure of a CoFe layer and a NiFe layer.

Thereafter, a metal line is formed by depositing a Ta film 21 and a Ru film 23 on the free ferromagnetic layer 19.

Fig. 2 is a graph illustrating the relationship between the resistance characteristic per unit area of MTJ cell and the minimum area of MTJ cell for implementation of the device.

Fig. 3 is a graph illustrating the relationship between the thickness of an alumina tunnel barrier layer, and the resistance characteristic per unit area of MTJ cell.

As described above, a conventional method for fabricating a MRAM is advantageous in fabricating a MRAM having high density because a MTJ occupying smaller area can be implemented as the resistance value per unit area of MTJ cell becomes lower as shown in Fig. 2 by forming the tunnel barrier layer using alumina.

However, when an insulating layer such as an alumina layer is used as a tunnel barrier layer, variations in the resistance "RA" of MTJ cell which is dependent on the thickness of alumina layer as shown in Fig. 3. As a result, it is difficult to satisfy a current process margin where the thickness variation of the alumina layer allowed within the limit of the resistance variation of a device must be less than 0.1nm.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for fabricating a MRAM wherein the electric conductivity of a tunnel barrier layer having a thickness 1 - 10 times greater than that of a conventional tunnel barrier layer is controlled by impurity concentration to

obtain sufficient process margin and improve characteristics, reliability, yield and productivity of a device.

In order to achieve the above object, there is provided a method for fabricating a MTJ cell of a MRAM, comprising the steps of: forming a pinned ferromagnetic layer on a connection layer; forming a tunnel barrier layer on the pinned ferromagnetic layer by depositing a semiconductor film; and forming a free ferromagnetic layer on the tunnel barrier layer.

It is preferable that the semiconductor film consists of a pure Group IV element.

It is also preferable that the semiconductor film consists of a Group IV element and includes a Group III element or a Group V element as an impurity.

It is also preferable that the semiconductor film is a compound semiconductor film consisting of a Group III element and a Group V element.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional diagram illustrating a MTJ cell structure of a conventional MRAM.

Figs. 2 and 3 are graphs illustrating characteristic variations of a MTJ cell.

Fig. 4 is a cross-sectional diagram illustrating a MTJ cell structure of a MRAM according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be explained in detail referring to the accompanying drawings.

Fig. 4 is a cross-sectional diagram illustrating a MTJ cell of a MRAM according to a preferred embodiment of the present invention.

Referring to Fig. 4, a lower insulating layer 31 is formed on a semiconductor substrate (not shown).

The lower insulating film 31 is an insulating film planarizing the entire surface of the semiconductor substrate having a device isolation film (not shown), a transistor (not shown) comprising a first wordline which is a read line and a source/drain region, a ground line (not shown), a conductive layer (not shown), and a second wordline (not shown) which is a write line thereon.

Then, a connection layer 33 electrically connected to the conductive layer is formed using Ta.

A pinned ferromagnetic layer 35 electrically connected to the connection layer 33 is formed.

The pinned ferromagnetic layer 35 includes a stacked

structure of a NiFe layer, a PtMn layer, a CoFe layer, a Ru layer and a CoFe layer.

Thereafter, a tunnel barrier layer 37 is formed on the pinned ferromagnetic layer 35. Preferably, the tunnel barrier layer 37 has a thickness ranging from 2 to 20nm.

Preferably, the tunnel barrier layer 37 is a semiconductor film consisting of a pure Group IV element. Group III or Group V elements such as B, P, As may be added to the tunnel barrier layer 37 consisting of a pure Group IV element for controlling electric conductivity. A compound semiconductor film consisting of a Group III element such as Ga or In and a Group V element such as As or P may be also used as the tunnel barrier layer 37.

Thereafter, a free ferromagnetic layer 39 is formed on the tunnel barrier layer 37.

The free ferromagnetic layer 39 includes a stacked structure of a CoFe layer and a NiFe layer.

A metal line is then formed on the free ferromagnetic layer 39 by depositing a Ta film 41 and a Ru film 43.

As discussed above, the improved method for fabricating a MTJ cell of a MRAM wherein the electric conductivity of a tunnel barrier layer having a thickness 1 - 10 times greater than that of a conventional tunnel barrier layer is controlled by impurity concentration to

obtain sufficient process margin and improve characteristics, reliability, yield and productivity of a device.